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10EC45

Fourth Semester B.E. Degree Examination, Dec.2018/Jan.2019
Fundamentals of HDL

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting atleast TWO questions from each part.***

PART – A

1 a. If A and B are two unsigned variables, with A = 1100 and B = 1001, find the value of following expressions:
(i) A and B (ii) A ^ B (iii) A && B
(iv) A >> 1 (v) ~ | A (vi) B ror 2 **(06 Marks)**

b. Explain verilog data types. **(08 Marks)**

c. Explain std_logic and bit_vector data types in VHDL. **(06 Marks)**

2 a. Write the gate level diagram and VHDL code of 2×2 bit combinational array multiplier in Data flow description style. Draw the simulation waveforms. **(10 Marks)**

b. Write the verilog code of 3 bit ripple carry adder in data flow description style. Assume 4 ns propagation delay for all gates. Draw the simulation waveform. **(10 Marks)**

3 a. Explain verilog repeat and forever statements with example. **(04 Marks)**

b. Write verilog code for positive edge triggered JK flip-flop in behavioral description style. **(06 Marks)**

c. Write the flow chart and VHDL code of Booth algorithm of multiplication. **(10 Marks)**

4 a. Write the structural description of 3-bit magnitude comparator using 3-bit adder in VHDL. **(10 Marks)**

b. Write the verilog description for 3-bit asynchronous down counter using generate. **(10 Marks)**

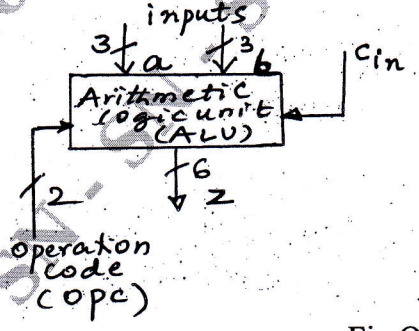
PART – B

5 a. Write VHDL code for converting a signed binary to integer using procedure. **(08 Marks)**

b. Write VHDL code for writing integers to a file. **(08 Marks)**

c. Write verilog function to find the greater of two signed numbers. **(04 Marks)**

6 a. Write the mixed type description of ALU in Fig.Q6(a) using verilog code. Addition is to be implemented by carry look ahead adder in data flow style. Multiplication and division by behavioral style. **(10 Marks)**



operation code (opc)	Operation
00	Addition
01	Multiplication
10	integer division
11	No operation

Fig.Q6(a)

b. Write VHDL code for 16×8 SRAM (Static memory) with block diagram and function table. Use package. **(10 Marks)**

7 a. Write mixed language description of a master slave D flip-flop invoking a VHDL entity for D latch from a verilog module. **(08 Marks)**
b. Write a mixed language description of an AND gate invoking a verilog module from a VHDL module. **(08 Marks)**
c. Discuss the limitations of mixed language description. **(04 Marks)**

8 a. Define synthesis. With flow chart, explain the steps involved in synthesis process. **(08 Marks)**
b. Write verilog code for signal assignment statement $y = 2 * x + 3$. Show the synthesized logic symbol and gate level diagram. Write structural code in verilog using gate level diagram. **(08 Marks)**
c. For the listing given draw the gate level diagram.

```
always @(a, x, x1)
  begin
    if (a = = 1'b1)
      y = x;
    else
      y = x1;
  end
```

(04 Marks)

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